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Description

[DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND BIT LINE PRECHARGE METHOD THEREFOR]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a dynamic semiconductor memory device and a bit line precharge method therefor. More particularly, the present invention relates to a dynamic random access memory (DRAM) that performs a refresh operation in a standby mode and a bit line precharge method .

[0003] Background of the Invention

[0004] Reducing power dissipation of integrated circuits in battery-driven equipment, such as a cellular telephone or a personal digital assistant (PDA), is a significant challenge. Previously, static random access memories (SRAMs) have been used extensively in semiconductor memory applica-

tions, because a SRAM memory cell typically has six complementary metal oxide semiconductor (CMOS) transistors and allows data to be retained with a minimal amount of current drain. In terms of area, however, the SRAM memory cell, is larger than a DRAM memory cell by a factor of twenty or more. In addition, memory capacities are increasing proportionately with circuit and wiring densities. As such, fabricating a 32-Mbit or 64-Mbit SRAM using current wiring technology of about 0.2 μm to about 0.13 μm inevitably results in an excessively large chip. Consequently, from the viewpoint of area efficiency, SRAMs are inferior to DRAMs, and the disadvantage of poor area efficiency ultimately inhibits continued process technology scaling. For this reason, in many applications SRAMs are being replaced by DRAMs.

SUMMARY OF INVENTION

[0005] Referring to Fig. 12, a conventional DRAM has a memory cell array 10 that includes memory cells (not shown) disposed in rows and columns, word lines WL disposed in rows, bit line pairs BL, /BL disposed in columns, a row decoder 12 that selectively activates the word lines WL, a sense amplifier 14 that amplifies a potential difference between paired bit lines BL, /BL, a half-Vdd regulator 16

that generates a voltage Vdd/2, which is half a line voltage Vdd, N-channel MOS transistors Q1 to Q3 for precharging the bit line pairs BL, /BL to Vdd/2, and a timing control circuit 18 that controls the sense amplifier 14 and the transistors Q1 to Q3.

[0006] The DRAM has a standby mode in addition to an active mode in which the DRAM reads/writes data. In the standby mode, the DRAM does not read or write data at all and performs only a refresh operation to retain currently stored data. The refresh operation is performed at a fixed interval (hereinafter referred to as "refresh cycle"). The refresh operation reads out data once from a memory cell and rewrites data to the memory cell, and it is basically similar to a normal read/write operation.

[0007] Still referring to Fig. 12, before the refresh operation, a precharge/equalize signal PC/EQ is at a logic high level, so that the transistors Q1 to Q3 are on, and the bit line pair BL, /BL is precharged to Vdd/2. When the timing control circuit 18 sets the precharge/equalize signal PC/EQ to a logical low level and the row decoder 12 activates the word line WL, data is read from a memory cell, causing a potential difference between the paired bit lines BL, /BL. Then, when the timing control circuit 18 sets a sense am-

plifier control signal SAC to a logic high level, the sense amplifier 14 is activated. The sense amplifier 14 amplifies the potential difference between the paired bit lines BL, /BL, and it raises one of the paired bit lines BL, /BL to the line voltage Vdd, while it lowers the other to a ground voltage GND. This causes data to be rewritten to a memory cell, thus refreshing the data in the memory cell. The timing control circuit 18 resets the sense amplifier control signal SAC to logic low and the row decoder 12 deactivates the word line WL, then the timing control circuit 18 resets the precharge/equalize signal PC/EQ to a logic high. This causes the bit line pair BL, /BL to be precharged to Vdd/2 again. The series of steps from the activation to the deactivation of the word line WL described above is referred to as the "refresh operation." For purposes of the following failure mode analysis, it is assumed that the word line WL is shorted with the bit line /BL by a defect at an intersection X in Fig. 12. Although such a bit line pair BL, /BL is electrically replaced by a redundant bit line pair RBL, /RBL, the bit line pair BL, /BL still physically exists. When the bit line pair BL, /BL is precharged to Vdd/2 while the voltage of the word line WL is at the ground voltage GND, leakage current Id is produced between the

bit line /BL and the word line WL. The half-Vdd regulator 16 is always activated, so that leakage current ID flows from the power source toward the ground via the half-Vdd regulator 16, the bit line /BL, and the word line WL. If the efficiency of the half-Vdd regulator 16 is denoted by Re, where (0<Re<1), then the leakage current ID is expressed by Id/Re.

[0008] Fig. 14 shows consumption current in the standby mode (hereinafter referred to as "standby current"). If a refresh cycle Tr is, for example, approximately 15.6 μs in duration, then the time actually required for refresh (hereinafter referred to as "refresh operating period") T1 is about 60 ns in a 0.2 μm technology. During the refresh operating period T1, a large alternating current AC is required to perform the refresh operation. Fig. 14 shows refresh current RF1 obtained by averaging the alternating current AC by the refresh operating period T1 and refresh current RF2 obtained by averaging the alternating current AC by the refresh cycle Tr. The alternating current AC required for refresh does not flow during a period of 15.54 μs (hereinafter referred to as "refresh non-operating period") T2 corresponding to 99.6% or more of the refresh cycle Tr. The DRAM, however, has various reference volt-

age generator circuits in addition to the half-Vdd regulator 16, in its peripheral circuit, so that direct current DC flows during the refresh non-operating period T2. In addition, the aforementioned leakage current ID also flows. Thus, the standby current ST is a sum of the direct current DC, the refresh current RF2, and the leakage current ID.

[0009] Since the leakage current ID is attributable to a defect, it is difficult to predict its value. For this reason, a sufficiently large value must be set as a standard value. Furthermore, the leakage current ID may be highly variable, making it difficult to reliably manufacture a DRAM with small leakage current ID over a long time. The leakage current ID may be as large as a few tens of μA for a DRAM in the range of a few tens of megabits, and even larger for a DRAM in the range of a few gigabits. It is hence predicted that the leakage current ID will be far larger than the refresh current RF2, posing a serious problem for a low-current DRAM aiming at standby current of about 10μA.

[0010] Japanese Unexamined Patent Application (PUPA) No. 5-128858 discloses a GND precharge method to prevent the leakage current caused by a short-circuit defect as described above. According to the GND precharge

method, bit line pairs are precharged to the same ground voltage as that of word lines, in contrast to the half-Vdd precharge method that precharges bit line pairs to Vdd/2. Although the leakage current can be substantially eliminated according to the GND precharge method because the bit line pairs share the same ground voltage as the word lines in the standby mode. However, in the active mode, the voltage of the bit line pairs must have a full amplitude between the ground voltage and the line voltage, meaning that a normal operating current will be double that in the half-Vdd precharge method. This leads to the conclusion that the GND precharge method is not effective for reducing consumption current.

[0011] An object of the present invention is to provide a dynamic semiconductor memory device capable of reducing standby current, and a bit line precharge method therefor.

[0012] Another object of the present invention is to provide a dynamic semiconductor memory device capable of reducing leakage current attributable to a defect without increasing normal operating current, and a bit line precharge method therefor.

[0013] The present invention discloses a dynamic semiconductor memory device that performs a refresh operation in a

standby mode, and has a plurality of bit line pairs, a precharger, a plurality of word lines, a row decoder, and a controller. The precharger precharges the bit line pairs to a voltage that is half a line voltage. The word lines cross bit line pairs. The row decoder selectively activates the word lines. The controller activates the precharger in the standby mode, during a predetermined period before the word lines are activated, while it deactivates the precharger in other periods.

[0014] A bit line precharge method in accordance with the present invention includes a step for precharging bit line pairs to a voltage that is half a line voltage during a predetermined period in the standby mode before the word lines are activated, and a step for electrically floating bit line pairs during a period other than the predetermined period.

[0015] According to the dynamic semiconductor memory device and the bit line precharge method therefor, the word lines are activated to perform the refresh operation in the standby mode. The bit line pairs are precharged during the predetermined period before the word lines are activated, but electrically floated (not precharged) during other periods. Hence, even if the word lines are shorted

with the bit lines, leakage current does not flow between the word lines and bit lines. This allows standby current to be reduced. In addition, the bit line pairs are precharged to a voltage that is half a line voltage, as in the conventional precharge method, so that normal operating current does not increase in an active mode.

Brief Description of Drawings

[0016] Fig. 1 shows a functional block diagram of a DRAM in accordance with a first embodiment of the present invention;

[0017] Fig. 2 illustrates a functional block diagram of an individual DRAM block;

[0018] Fig. 3 shows a timing chart corresponding to a refresh operation of the DRAM shown in Figs. 1 and 2;

[0019] Fig. 4 illustrates a functional block diagram of a partial configuration of a DRAM according to a second embodiment of the present invention;

[0020] Fig. 5 shows a timing chart corresponding to a refresh operation of the DRAM shown in Fig. 4;

[0021] Fig. 6 illustrates a functional block diagram of a partial configuration of a DRAM according to a third embodiment of the present invention;

[0022] Fig. 7 shows a timing chart corresponding to a refresh

operation of the DRAM shown in Fig. 6;

[0023] Fig. 8 shows a timing chart corresponding to a DRAM refresh operation according to a fourth embodiment of the present invention;

[0024] Fig. 9 illustrates a partial configuration block diagram of a DRAM according to a fifth embodiment of the present invention;

[0025] Fig. 10 shows a timing chart corresponding to a refresh operation of the DRAM shown in Fig. 9;

[0026] Fig. 11 shows a timing chart corresponding to a DRAM refresh operation according to a sixth embodiment of the present invention;

[0027] Fig. 12 illustrates a functional block diagram of a partial configuration of a conventional DRAM;

[0028] Fig. 13 shows a timing chart corresponding to a refresh operation of the DRAM shown in Fig. 12; and

[0029] Fig. 14 depicts a waveform diagram showing consumption current in a standby mode of the DRAM shown in Fig. 12.

DETAILED DESCRIPTION

[0030] Embodiments according to the present invention will now be explained in detail with reference to the accompanying drawings. Like or equivalent elements will be assigned like reference numerals or characters and the descriptions

thereof will be reused.

[0031] Referring to Fig. 1, a DRAM in accordance with the first embodiment has a memory cell array 20, a half-Vdd regulator 16, a row address receiver 24, a timer 26, a row address counter 28, and a selector 30. The memory cell array 20 is divided into a plurality of blocks 22. The half-Vdd regulator 16 generates a voltage Vdd/2, which is half a line voltage, and supplies it to the memory cell array 20.

[0032] Referring to Fig. 2, each block 22 includes a memory cell array 10 that has memory cells (not shown) arranged in rows and columns, a plurality of word lines WL disposed in rows, a plurality of bit line pairs BL, /BL that are disposed in columns and cross the word lines WL, a row decoder 12 that selectively activates the word lines WL in response to a predecode signal PD, a sense amplifier 14 that amplifies a potential difference between a bit line BL and a bit line /BL, transistors Q1 to Q3 for precharging the bit line pairs BL, /BL to Vdd/2, and a timing control circuit 18 for controlling the sense amplifier 14 and the transistors Q1 to Q3.

[0033] The transistor Q1 is connected between the bit line BL and the bit line /BL. The transistor Q2 is connected between the bit line BL and a half-Vdd line 32. The transistor Q3 is

connected between the bit line /BL and the half-Vdd line 32. The half-Vdd line 32 is connected to an output end of the half-Vdd regulator 16. A precharge/equalize signal PC/EQ is commonly supplied to the gates of transistors Q1 to Q3. The transistors Q1 to Q3 turn on/off in response to the precharge/equalize signal PC/EQ.

[0034] Referring back to Fig. 1, the row address receiver 24 receives an input external row address signal ERA. The timer 26 supplies a refresh enable signal RE to the row address counter 28 and the selector 30 in a predetermined refresh cycle (e.g., 15.6 μs). The row address counter 28 generates and retains an internal row address signal IRA. The internal row address signal IRA is incremented in response to the refresh enable signal RE. In a normal access mode, the selector 30 selects the external row address signal ERA from the row address receiver 24. In a standby mode, the selector 30 selects the internal row address signal IRA from the row address counter 28 in response to the refresh enable signal RE.

[0035] The row address signal ERA or IRA selected by the selector 30 is supplied to a predecoder (not shown) in the memory cell array 20. The predecoder translates the row address signal ERA or IRA, and supplies a predecode signal PD to

the row decoder 12 and a block enable signal BE to the timing control circuit 18. The timing control circuit 18 is activated in response to the block enable signal BE, and selects the block 22.

[0036] The refresh operation of the DRAM in the standby mode is shown in Fig. 13. The conventional precharge/equalize signal PC/EQ continuously remains at a logic high level during the period from the moment the word lines WL are deactivated to the moment they are activated. The precharge/equalize signal PC/EQ in accordance with the present embodiment transitions to a logic high only during a predetermined period Tpc before the word lines WL are activated, while it is maintained at a logic low during other periods, as shown in Fig. 3.

[0037] When the timing control circuit 18 sets the precharge/equalize signal PC/EQ to a logic high, the transistors Q1 to Q3 turn on at the same time. This causes the bit line pairs BL, /BL to be connected to the half-Vdd line 32 and also causes the bit line BL and the bit line /BL to be shorted with each other, thus precharging the bit line pair BL, /BL to Vdd/2.

[0038] When the precharge/equalize signal PC/EQ returns to a logic low, the row decoder 12 activates the word line WL.

When the voltage of the word line WL rises to a level higher than the line voltage Vdd, data is read from a memory cell, producing a potential difference between the paired bit lines BL, /BL. When the timing control circuit 18 sets a sense amplifier control signal SAC to a logic high, the sense amplifier 14 is enabled. The sense amplifier 14 raises the voltage of a higher-bit line to the line voltage Vdd, while it lowers the voltage of a lower-bit line to a ground voltage GND. This causes data to be rewritten to the memory cell, thereby accomplishing the refresh operation.

[0039] Subsequently, the timing control circuit 18 sets the sense amplifier control signal SAC to a logic low, the row decoder 12 deactivates the word line WL, and the voltage of the word line WL returns to ground potential GND. As soon as the word line WL is deactivated, the conventional precharge/equalize signal PC/EQ switches to a logic high, whereas the precharge/equalize signal PC/EQ according to the present embodiment remains at a logic low level. Hence, the bit line pair BL, /BL will not be precharged and is maintained in an electrically floated state. This causes the voltage Vdd of the higher-bit line to gradually decrease toward the ground voltage GND.

[0040] Then, the timing control circuit 18 again sets the precharge/equalize signal PC/EQ to a logic high but only for the predetermined period Tpc before the word line WL is activated.

[0041] According to the present embodiment, even if the word line WL is shorted with the bit line /BL at an intersection X shown in Fig. 2, the precharge/equalize signal PC/EQ remains at a logic low for a period other than the predetermined period Tpc. Thus, the bit line pair BL, /BL is disconnected from the half-Vdd line 32 and therefore not precharged to Vdd/2. Unlike the conventional case, leakage current does not flow between the bit line /BL and the word line WL. Moreover, the present embodiment employs the half-Vdd precharge method in which the bit line pairs BL, /BL are precharged to Vdd/2, as in the conventional case, thus obviating the need for full amplitude of the voltage of the bit line pairs BL, /BL between the ground voltage GND and the line voltage Vdd. Hence, unlike the GND precharge method in which the bit line pairs BL, /BL are precharged to the ground voltage GND, active current will not increase, permitting an effective reduction of standby current to be achieved.

[0042] However, additional precharge current is required to

precharge the bit line pairs BL, /BL from the ground voltage GND to Vdd/2 before refresh. It is therefore preferable to perform a burst refresh rather than carrying out single refresh at predetermined refresh intervals (e.g., 15.6 μs).

[0043] If, for example, a refresh operation period of time per word line is 60 ns in a case where 16 word lines are successively activated in order in one burst refresh, then one burst refresh takes 960 ns (= 60 ns x 16). If the burst refresh is carried out sixteen times at 15.6-μs refresh intervals, then the sixteen burst refresh operations will take 249.6 μs (= 15.6 μs x 16).

[0044] Such burst refresh operations do not require precharging the bit line pairs immediately before activating word lines. This means that precharging the bit line pairs only immediately before the first activation of the word lines and omitting the precharge of the bit line pairs immediately before the activation of the subsequent word lines will significantly reduce precharge current. More specifically, the precharge current will be 1/16 of the conventional DRAM current when the burst refresh operation is performed 16 times, or 1/32 conventional DRAM current when the burst refresh operation is performed 32 times.

[0045] If a 0.2 μm CMOS technology is used, the typical bit-line capacitance is 100 fF, Vdd/2 = 0.75 V, and the number of bit line pairs is 4K (= 4 x 1024), then precharge current Ip required for precharging the bit line pairs from the ground voltage to Vdd/2 is given by the following expression:Ip = 100fF x 2 x 4 x 1024 x 0.75V/15.6μs = 39μA When the burst refresh operation is performed 16 times, the precharge current will be Ip=39μA/16=2.4μA. When the burst refresh operation is performed 32 times, the precharge current will be Ip=39μA/32=1.2μA.

[0046] Thus, an increase in the precharge current Ip is small, as compared with a case where the leakage current caused by a defect exceeds a few tens of μA.

[0047] The invention according to a second embodiment is shown in Fig. 4. A timing control circuit 18 issues two discrete signals for the equalize signal EQ and precharge signal PC functions. This approach differs from the first embodiment described above in that the precharge PC and equalize EQ signals are combined. The equalize signal EQ is commonly supplied to the gates of transistors Q1, and the precharge signal PC is commonly supplied to transistors Q2 and Q3. Referring to Fig. 5, the equalize signal EQ changes in the same manner as the conventional

precharge/equalize signal PC/EQ (Fig. 13), and the precharge signal PC changes in the same manner as the precharge/equalize signal PC/EQ (Fig. 3) in the aforementioned first embodiment.

[0048] When the word line WL is deactivated, the equalize signal EQ transitions to a logic high level, whereas the precharge signal PC remains low. When the equalize signal EQ transitions a logic high level, the transistor Q1 turns on, causing a bit line BL and a bit line /BL to be shorted with each other. Since the precharge signal PC remains at a logic low, the transistors Q2 and Q3 remain off. Thus, a bit line pair BL, /BL is floated and not precharged by a half-Vdd regulator 16. Accordingly, even if the word line WL is shorted with the bit line /BL at an intersection X shown in Fig. 4, no leakage current flows between the bit line /BL and the word line WL.

[0049] The precharge signal PC is set to a logic high for a predetermined period Tpc before the word line WL is activated. At this time, the equalize signal EQ maintains a logic high level. When the precharge signal PC is set to a logic high, the transistors Q2 and Q3 turn on, causing the bit line pair BL, /BL to be precharged to Vdd/2 by the half-Vdd regulator 16. When the equalize signal EQ and the

precharge signal PC are both reset to a logic low, the voltage of the word line WL increases.

[0050] As described above, according to the second embodiment, the precharge signal PC is set to a logic low outside the period Tpc immediately before the word line WL is activated, and the bit line pair BL, /BL is disconnected from the half-Vdd line 32. This arrangement prevents leakage current attributable to a defect from flowing, thus achieving a substantially reduced standby current.

[0051] A third embodiment, shown in Fig. 6, provides a dummy word line DWL along a standard word line WL. The dummy word line DWL is normally provided at an end of a memory cell array 10 to maintain the regularity of layout, and not intended to be used for reading or writing data. In the present embodiment, the dummy word line DWL is activated to perform a dummy read operation.

[0052] More specifically, a timing control circuit 18 sets an equalize signal EQ to a logic high level during a predetermined period Tpc immediately before activating the word line WL, and always maintains a precharge signal PC at a logic low level in the standby mode, as illustrated in Fig. 7. A row decoder 12 activates the dummy word line DWL before activating the word line WL. In this case, since no

actual data reading is performed, the row decoder 12 has to raise the voltage of the dummy word line DWL only as high as a line voltage Vdd, and does not have to boost it more than the line voltage Vdd. While the dummy word line DWL is being activated, the timing control circuit 18 sets a sense amplifier control signal SAC to a logic high level.

[0053] When the dummy word line DWL is activated, data is read from a dummy memory cell (not shown) connected to the dummy word line DWL to a bit line pair BL, /BL. The data, which may be any data, causes a potential difference between the paired bit lines BL, /BL. When the sense amplifier control signal SAC goes high, a sense amplifier 14 is activated, amplifying the abovementioned potential difference. This raises the voltage of a higher-bit line to the line voltage Vdd, while it reduces the voltage of a lower-bit line to the ground voltage GND.

[0054] When the equalize signal EQ goes high after the sense amplifier control signal SAC returns to a logic low and the voltage of the dummy word line DWL is set back to the ground voltage GND, the transistor Q1 turns on, causing the bit line BL and the bit line /BL to be shorted with each other. This equalizes the voltage of the bit line pair BL, /

BL to Vdd/2. After the equalize signal EQ falls to a logic low, the voltage of the word line WL rises.

[0055] As described above, according to the third embodiment, the precharge signal PC is always maintained low in the standby mode to disconnect the bit line pairs BL, /BL from the half-Vdd line 32, thus preventing leakage current attributable to a defect from flowing. As a result, the standby current can be reduced. Although the precharge signal PC is always maintained at a logic low in the standby mode, the bit line pairs BL, /BL can be precharged to Vdd/2 since the dummy word line DWL is enabled and the sense amplifier 14 is activated before the word line WL is enabled.

[0056] The timing diagram corresponding to a fourth embodiment is shown in Fig. 8. Note that the dummy read operation described in the third embodiment is performed using the dummy word line DWL to precharge the bit line pairs BL, /BL to Vdd/2. If, however, no dummy word line DWL is provided, then the sense amplifier 14 may simply be activated. More specifically, as shown in Fig. 8, a timing control circuit 18 sets a sense amplifier control signal SAC to a logic high immediately before the voltage of the bit line pair BL, /BL is equalized.

[0057] If a sense amplifier control signal SAC goes high when none of the word lines WL have been enabled, the sense amplifier 14 is activated. At this time, no data is read from the bit line pair BL, /BL, but a slight potential difference naturally exists between the paired bit lines BL, /BL. The sense amplifier 14 amplifies the potential difference to raise the voltage of the higher-bit line to the line voltage Vdd and to reduce the voltage of the lower-bit line to the ground voltage GND. The bit line pair BL, /BL are equalized and precharged to Vdd/2 when the equalize signal EQ goes high after the sense amplifier control signal SAC returns to a logic low to deactivate the sense amplifier 14.

[0058] A fifth embodiment, shown in Fig. 9, provides a power line 34 and a grounding conductor 36 in place of the half-Vdd regulator 16 in the previously described embodiments. A line voltage Vdd is supplied to the power line 34, and a ground voltage GND is supplied to the grounding conductor 36. A P-channel MOS transistor Q4 is connected between the power line 34 and a bit line BL. An N-channel MOS transistor Q5 is connected between the grounding conductor 36 and a bit line /BL. A precharge signal PCP is commonly supplied to the gates of a plurality of transistors Q4. A precharge signal PCN is commonly supplied to

the gates of a plurality of transistors Q5. The transistors Q4 turned on/off in response to the precharge signal PCP, and the transistors Q5 turn on/off in response to the precharge signal PCN.

[0059] A timing control circuit 18 sets an equalize signal EQ high during a predetermined period Tpc1 immediately before a word line WL is enabled, as shown in Fig. 10. The timing control circuit 18 further sets the precharge signal PCP low and sets the precharge signal PCN high during a predetermined period Tpc2 immediately before the equalize signal EQ switches high.

[0060] When the precharge signal PCP goes low, the transistor Q4 turns on, causing one bit line BL to be connected to the power line 34 so as to be precharged to the line voltage Vdd. At the same time, when the precharge signal PCN switches high, the transistor Q5 turns on, causing the other bit line /BL to be connected to the grounding conductor 36 so as to be precharged to the ground voltage GND. When the precharge signal PCP returns to a logic high, while the precharge signal PCN returns to a logic low, and the equalize signal EQ switches high, the bit line pair BL, /BL is equalized and precharged to Vdd/2. In other words, one bit line BL is temporarily connected to

the power line 34 and the other bit line /BL is temporarily connected to the grounding conductor 36. After the bit line pair BL, /BL is isolated from the power line 34 and the grounding conductor 36, one bit line BL and the other bit line /BL are shorted with each other.

[0061] As described above, according to the fifth embodiment, the precharge signal PCP is set high and the precharge signal PCN is set low to disconnect the bit line pair BL, /BL from the power line 34 and the grounding conductor 36 during a period other than the predetermined period Tpc2 before the word line WL is enabled. This prevents the flow of leakage current attributable to a defect from occurring. As a result, the standby current can be significantly reduced. In addition, the absence of the half-Vdd regulator 16 contributes to a reduction in power consumption.

[0062] A timing diagram corresponding to a sixth embodiment is shown in Fig. 11. In the previous embodiment, the voltage of the bit line pair BL, /BL exhibits full amplitude swing between the ground voltage GND and the line voltage Vdd each time before the word line WL is activated. However, this is unnecessary in a burst refresh operation in which all word lines WL in the memory cell array 10 are successively activated in order. As shown in Fig. 11, the voltage

of the bit line pair BL, /BL attains full amplitude only before a first word line WL1 is activated, but no longer has full amplitude preceding the activation of subsequent word lines WL2 to WL256.

[0063] To be more specific, a timing control circuit 18 sets a precharge signal PCP low and a precharge signal PCN high during a predetermined period Tpc2 before the first word line WL1 is enabled. This causes the voltage of the bit line pair BL, /BL to have full amplitude, and one bit line BL is precharged to a line voltage Vdd, while the other bit line /BL is precharged to the ground voltage GND. Subsequently, when the equalize signal EQ goes high, the bit line pair BL, /BL is equalized and precharged to Vdd/2.

[0064] Hitherto, if a word line WL was shorted with the bit line /BL at with resistance of 5 kΩ and if Vdd=1.6V, then Id=1.6V/2/5kΩ=160μA. Furthermore, if Re=0.8, then ID=160μA/0.8=200μA. Accordingly, if there are any such defects, the requirements of a low-current DRAM cannot be satisfied.

[0065] According to the sixth embodiment, if, for example, Vdd is 1.6 V, the number of word lines is 256, a sense amplifier is activated for 10 ns, and the retention time during which a memory cell can hold data is 64 ms, then an in-

crease in DC current in a standby mode will be controlled to 0.013 μA (= 1.6V/5kΩ x 256 x 10ns/64ms). Hence, even if there are 100 defects, such as the ones mentioned above, an increase in the DC current will be 1.3 μA. This makes it possible to fabricate low-current DRAMs with higher yields without the need for paying much attention to defects.

[0066] While the invention has been described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is understood that numerous other modifications and variations can be devised without departing from the scope of the invention.